IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 22-23 and AMEND claims 24, 26, and 43 in accordance with the following:

Claims 1-23. (Cancelled)

24. (Currently Amended) An arrangement, comprising:

a substrate;

an electrical component arranged on a surface section of the substrate, the electrical component having an electrical contact surface; and

an electrical contact lug including

an electrically-conductive film having an electrical connection surface in electrical contact with the electrical contact surface of the electrical component, and

an area protruding beyond the electrical contact surface of the electrical component,

wherein the electrically-conductive film is a laminated interconnect having two electrical conductor layers and an electrical insulation layer arranged between the two electrical conductor layers, and

~~An arrangement in accordance with claim 23,~~ wherein the two electrical conductor layers and the electrical insulation layer of the laminated interconnect are arranged to produce opposing magnetic fields in the two electrical conductor layers upon electrical activation.

25. (Previously Presented) An arrangement according to claim 24, wherein the two electrical conductor layers of the laminated interconnect are substantially in a coplanar arrangement.

26. (Currently Amended) An arrangement ~~in accordance with~~ according to claim 25, wherein the electrical component is a power semiconductor chip.

27-42. (Cancelled)

43. (Currently Amended) An electronic device, comprising:

a substrate;

a power semiconductor chip arranged on a surface section of the substrate, the power semiconductor chip having an electrical contact surface; and

an electrical contact lug having

a laminated interconnect as an electrically-conductive film in electrical contact with the electrical contact surface of the power semiconductor chip, the laminated interconnect having at least two electrical conductor layers, which are substantially in a coplanar arrangement, and at least one electrical insulation layer arranged between the at least two electrical conductor layers, the at least two electrical conductor layers and the at least one electrical insulation layer being arranged to produce opposing magnetic fields in the at least two electrical conductor layers upon electrical activation, and

an area extending beyond the electrical contact surface of ~~said~~ the power semiconductor chip~~electrical component~~.